Saturated Resistor Load for GaAs Integrated Circuits

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Abstract—**Saturated resistors, two-terminal load devices, have been fabricated and evaluated as pull-up loads for GaAs digital integrated circuits. The saturated resistor loads exhibit superior device characteristics compared with FET active loads. Up to 100-percent improvement in the uniformity of the saturation current has been obtained. Ring oscillators with saturated resistor pull-up loads have shown ~20-percent lower speed-power products than ring oscillators with FET active loads. This superior circuit performance is attributed to 1) no gate capacitance, and 2) less backgating effect. Reliability studies using accelerated aging have shown that circuits are more reliable when saturated resistor loads are used.**

I. Introduction

IN AN INTEGRATED circuit, the load devices play very important roles in both the functionality and the performance of the circuit. Typically, active loads with nonlinear current saturation characteristics are used to provide fast and power-saving switching operations. In GaAs digital integrated circuits, regardless of the circuit approach one may select, Schottky diode FET logic (SDFL), directly coupled FET logic (DCFL), or buffer FET logic (BFL), nearly half of the circuit components are active loads. Usually an active load is constructed from a depletion-mode FET with its gate connected (shorted) to its source. Therefore, it is fabricated and designed like a three-terminal device, although it only provides a two-terminal function. A simpler and more natural approach would be to use a two-terminal device, as shown in Fig. 1, to achieve the desired current saturation characteristics. It has been reported that in GaAs this resistor structure can indeed provide a saturation characteristic and be used as a current stabilizer [1] and a load device [2]. The current saturation in this structure is obtained from the velocity saturation of the carriers. The low saturation field in GaAs (~3 kV/cm compared to ~20 kV/cm in Si) makes it possible to fabricate these saturated resistors with practical dimensions and use them effectively in integrated circuits operating at low voltages. In this paper, we report on the fabrication of saturated resistors using our planar technology [3] and on their electrical characteristics. Comparisons of device characteristics, circuit performance, and thermal reliability between circuits with FET active loads and circuits with saturated resistor loads are also presented.

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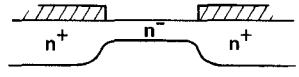

Fig. 1. A schematic drawing of the cross section of a saturated resistor.

II. Device Fabrication

The fabrication of a saturated resistor is compatible with our standard wafer processing which utilized planar selective ion-implantation techniques [3]. The structure of the saturated resistor, shown in Fig. 1, is similar to a FET without the Schottky gate. The n^- channel is obtained by the same Se implantation as the FET channel. An additional n^+ Si implantation under the ohmic contact regions is the same as that used in the source and the drain of the FET's for minimizing the contact resistance. The surface of the device is protected by a Si_3N_4 film and the two electrodes are alloyed AuGe/Ni contacts. The spacing between the n^+ regions is typically 2.5 μm.

Since Schottky gates are not used in the saturated resistors, potential problems encountered during fabrication of short gate FET's such as metal bridging, gate dimensional control, broken gate, etc., are not present. Higher process yield resulting from using such a simple resistor structure should greatly benefit the fabrication of dense and highly complex LSI/VLSI circuits.

III. Device Characteristics

Typical I–V characteristics of saturated resistors with three different widths (1 μm, 2 μm, and 3 μm) are shown in Fig. 2. Good saturation characteristics are obtained even with 1-μm wide devices. The saturation voltage is typically 1 V with 2.5-μm spacing between the n^+ implanted electrodes. Because there is no depletion region associated with a Schottky gate, a saturated resistor has a thicker current conduction path than a FET. The measured saturation current is more than two times higher than the saturation current (I_{DSS}) of a same-sized FET. This higher current carrying capability results in space saving and allows the fabrication of denser GaAs integrated circuits. The 1-V saturation voltage is adequate for most of our circuits. Lower saturation voltage may be obtained by reducing the gap between the two electrodes. However, one has to be

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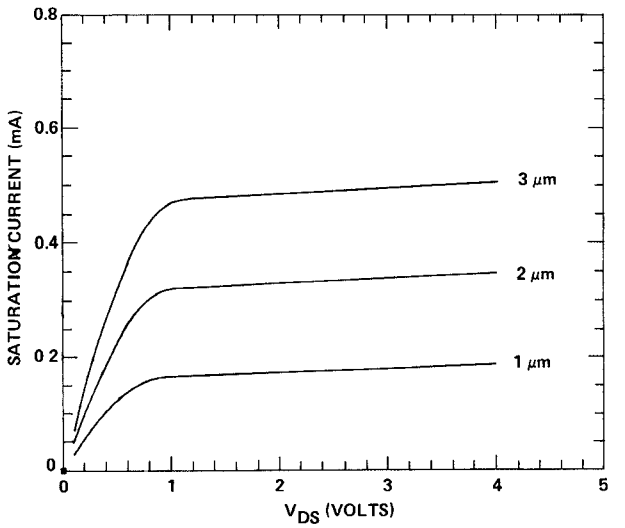


Fig. 2. Current–voltage characteristics of three saturated resistors with width equal to 1 μm, 2 μm, and 3 μm.

careful when fabricating very short-gap structures since the saturation current can increase and the output resistance can decrease due to a combination of lateral diffusion of n^+ dopants in the channel and substrate leakage between electrodes.

The current saturation mechanism of a saturated resistor is based on the velocity saturation of carriers at high fields. Assuming a uniformly doped channel active layer, the saturation current is

$$I_S = wqnv_s a \propto na \tag{1}$$

where w is the width of the device, q is the electronic charge, n is the carrier concentration, v_s is the saturation velocity, and a is the depth of the active layer. Since the saturation velocity v_s is independent of process variations, the saturation current is only proportional to the product of n and a. In contrast, the current saturation mechanism of a low-threshold FET is mainly controlled by the Schottky gate. The saturation current at zero gate to source voltage is given by [4]

$$I_{DSS} = KV_T^2 = \frac{w\mu\epsilon}{2aL_g}\left[V_B - \frac{nqa^2}{2\epsilon}\right]^2 \cdot \alpha \frac{V_B^2}{aL_g} + \frac{q^2n^2a^3}{4\epsilon^2 L_g} - \frac{nqaV_B}{\epsilon L_g} \tag{2}$$

where V_T is the threshold voltage of the FET, μ is the electron mobility, ϵ is the permittivity of GaAs, V_B is the built-in potential of the Schottky gate, and L_g is the gate length. The saturation current I_{DSS} is much more dependent on the process variations than the saturation current of a saturated resistor. Any variations in process parameters such as the Schottky barrier height of the gate metal, the gate length, and the implant profile parameters a and n, will result in much larger nonuniformity in the FET saturation currents than in the saturated resistor currents.

Experimentally we have observed up to 100-percent improvement in the current uniformity of saturated resistors

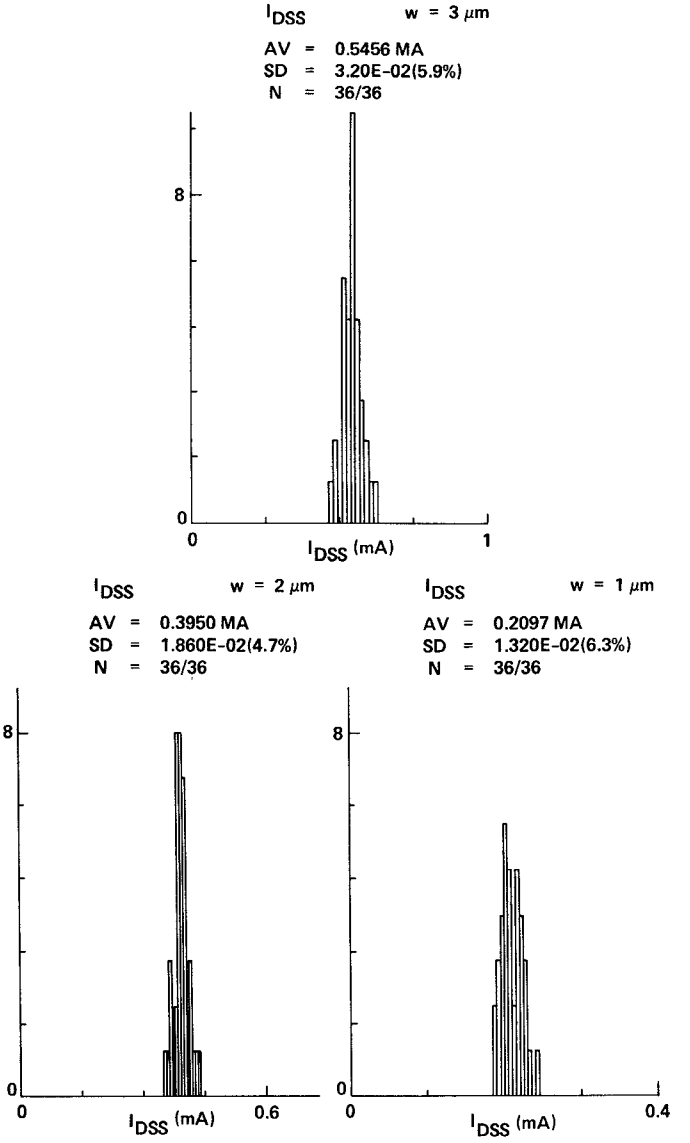
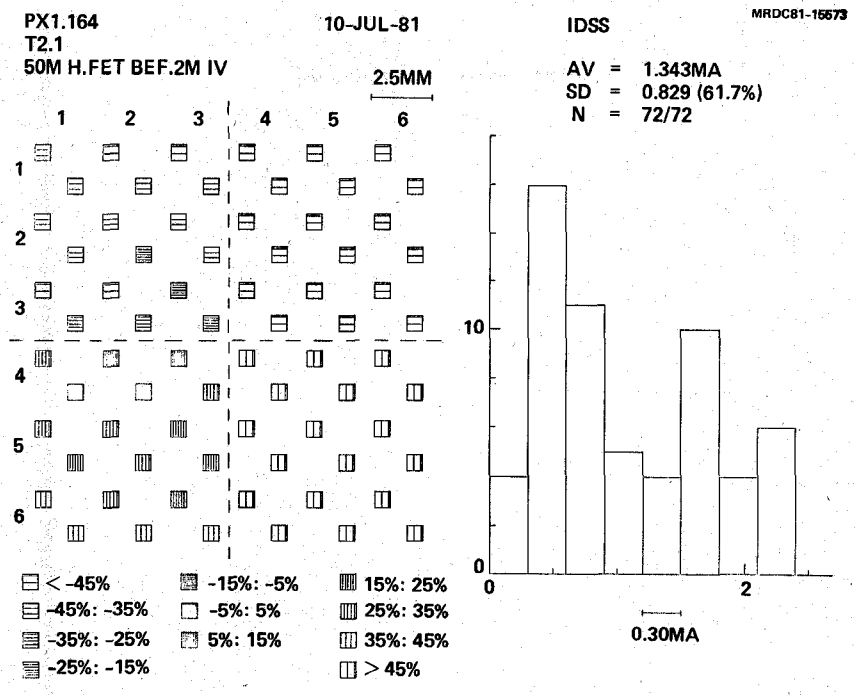
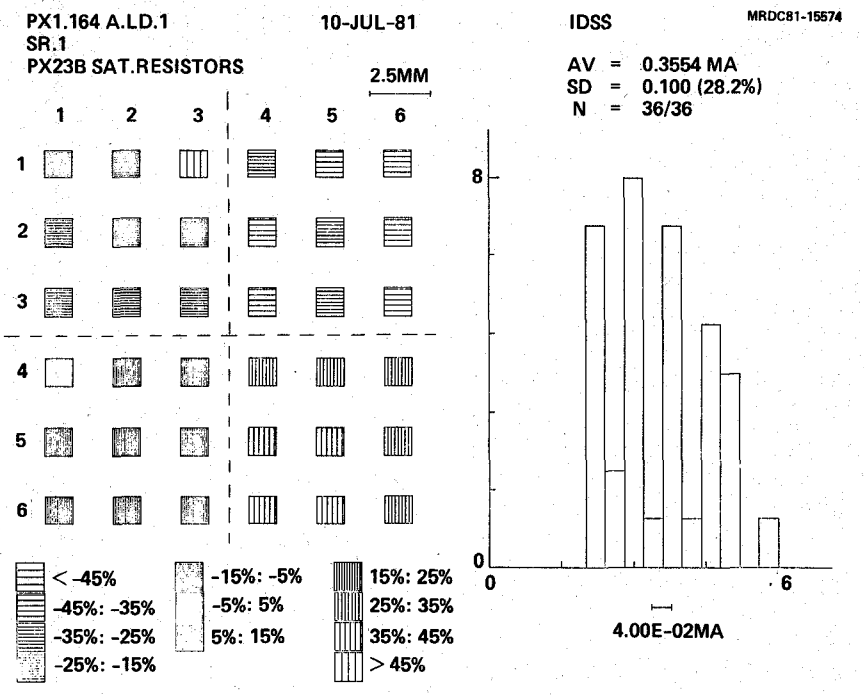


Fig. 3. Histograms of the saturation current distribution of saturated resistors with width equal to 1 μm, 2 μm, and 3 μm. Each graph consists of data obtained from 36 devices uniformly distributed across a 1-inch-square wafer.

over FET's. Fig. 3 shows the wafer histograms of saturation current for arrays of 36 1-μm, 2-μm, and 3-μm wide saturated resistors on the same one-inch-square wafer. The histograms show ~5.6-percent standard deviation in the saturation current for all three size resistors measured. From the data acquired from 14 wafers, an average of 92-percent improvement in the current uniformity of saturation resistors over FET's has been obtained. To illustrate this advantage in current uniformity an experiment was carried out using different ion-implanted doses in separate quadrants of a wafer to purposely create a large difference in the implanted profiles. The saturation currents of the FET's and the saturated resistors were then measured and compared. Fig. 4(a) and 4(b) are the maps and the histograms of the current distributions. The saturation current of the FET's, shown in Fig. 4(a), has a standard deviation of 61.7 percent, while the saturation current of the saturation resistors, shown in Fig. 4(b), has



(a)



(b)

Fig. 4. Map and histogram for the saturation current of (a) 50-μm FET's and (b) 3-μm saturated resistors. The wide spread in current distribution is due to different implant dose in each quadrant of the wafer.

only 28.2-percent standard deviation. In this experimental worst case, more than 100-percent improvement in the current uniformity was obtained.

Because the current for the saturated resistors is higher than that of the FET active loads with the same geometry, one has to use a smaller width saturated resistor to replace a FET load. In many situations, very small saturated resistors are required. Therefore, it is necessary to know how the saturation current scales with the width of the resistor when it is small. Fig. 5 shows the average saturation currents of 1-μm, 2-μm, and 3-μm wide saturated resistors which are uniformly distributed across a wafer. Each point on the curve represents the average current for 36 devices; the error bar indicates the standard deviation of the current. A straight-line scaling relation is obtained even for devices down to 1 μm wide. The straight line

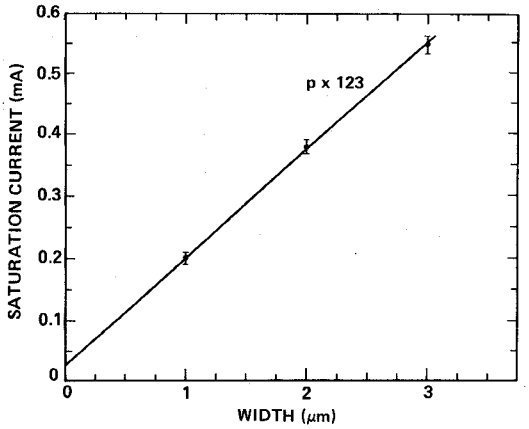


Fig. 5. The relation between the saturation current and the width of the saturated resistor.

intersects the horizontal axis at $x \simeq -0.25$ μm, indicating that the actual width of the device is about 0.25 μm wider than the designed value due to photolithographic line width control.

IV. Circuit Performance

A. Ring Oscillator Performance

The impact of the load design on circuit performance was studied using SDFL ring oscillators. Shown in Fig. 6 are two kinds of 9-stage ring oscillators containing 10-μm wide, 1-μm long gate switching FET's, and 2-μm pull-down FET active loads. The only difference between these ring oscillators is in the pull-up loads. One had 8-μm wide FET active loads and the other had 3-μm wide saturated resistor loads as indicated in the photograph of Fig. 6.

The circuits were tested on wafers with FET's exhibiting about 1-V threshold voltages. The positive power supply voltage V_{DD} was fixed at 2 V, and the negative power supply V_{SS} was varied from -0.5 V to about -2.5 V. The gate propagation delay τ, the pull-up current I_{DD}, and the pull-down current I_{SS}, were measured as functions of V_{SS}. Comparison of performance of two ring oscillators with different pull-up load structures is shown in Fig. 7. Both circuits operated at almost identical current values, indicating equivalent power levels, but the ring oscillator with saturated resistor loads exhibited about 20 percent lower propagation delays than the ring oscillator with FET pull-up loads. Gate propagation delays in the range of 60–90 ps were obtained for the circuit with saturated resistor loads comparing to the 80–130-ps propagation delays for the circuit with FET active loads. This improvement in speed is mainly attributed to the fact that saturated resistor loads have no gate capacitance and are less sensitive to backgating effects (discussed in the next section). The switching speed might be further increased if the pull-down FET's are also replaced by saturated resistors. However, because the size of the pull-down FET is already very small (2 μm), the fabrication of even smaller (<1 μm) saturated resistor pull-downs would be very difficult and has not yet been attempted.

We have also fabricated ring oscillators with the two types of pull-up loads designed in such a way that they operated at the same speed. In this case, we have seen that the circuit with saturated resistor loads consumed about 20 percent less power than the circuits with FET active loads. Therefore, it appears that regardless of whether we match the operating speed or the power consumption for the two types of pull-ups, the speed-power product of circuits with saturated resistor loads is always about 20 percent better than that of circuits with FET active loads.

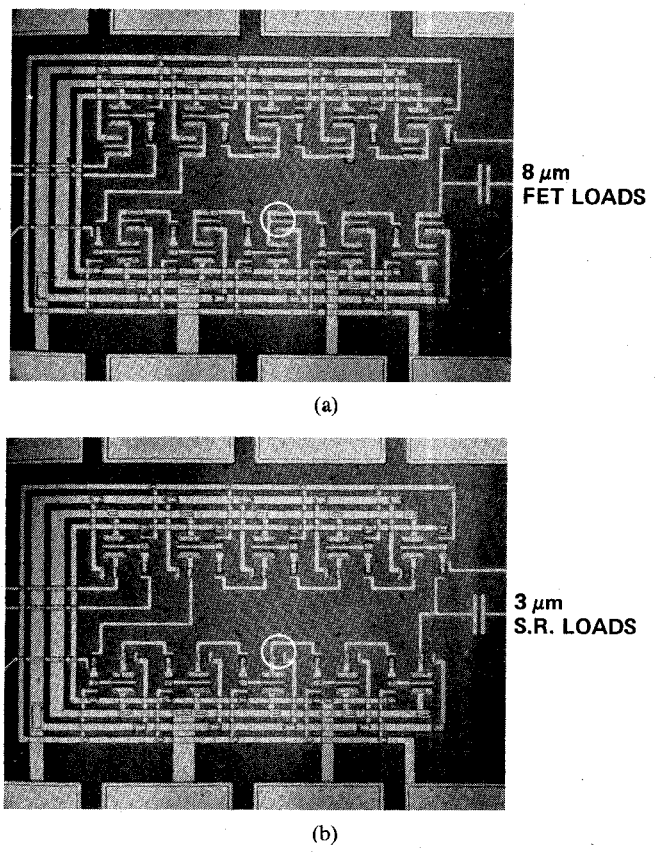


Fig. 6. Photographs of ring oscillators with (a) FET pull-up loads and (b) saturated resistor pull-up loads. The loads are indicated in the white circles.

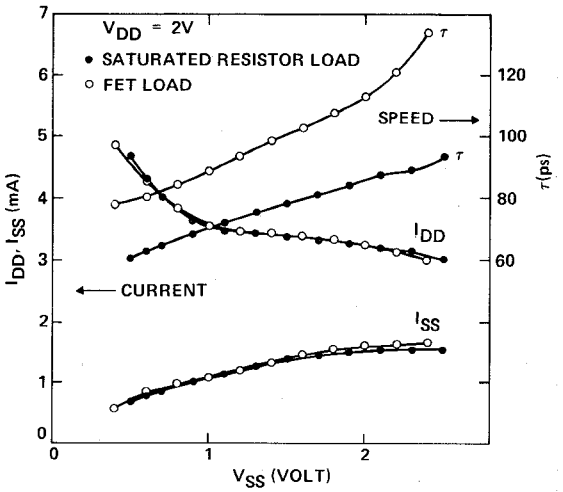


Fig. 7. Comparison between performances of two ring oscillators with different pull-up loads. With the same power consumption level the circuit with saturated loads is 20 percent faster than the circuit with FET active loads.

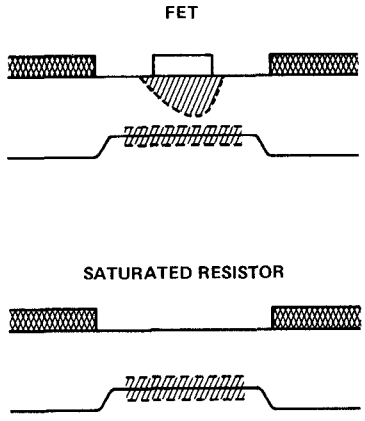


Fig. 8. Structural comparison between a FET and a saturated resistor. The shaded areas are the space charge regions.

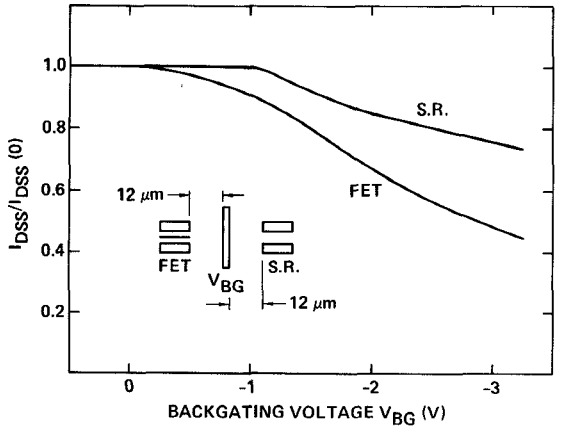


Fig. 9. Comparison of backgating characteristics between a FET and a saturated resistor. The normalized saturation currents are plotted against the backgating voltage applied to the ohmic finger.

B. Backgating Characteristics

Because the high resistivity of semi-insulating GaAs is obtained by impurity compensation, a space charge region exists at the active channel-substrate interface. The device characteristics can be influenced through the modulation of the space charge region by the negative voltage applied to the adjacent devices [5], [6]. This so-called backgating effect can degrade device performance and prevent optimal circuit operation. Backgating in a FET is different from the backgating in a saturated resistor. This can be explained by the device structures shown in Fig. 8. In a saturated resistor, because there is no space charge region due to the Schottky gate, the effective current conduction path is much thicker than that of a FET. The backgating effect, which comes from the modulation of the space charge region at the channel-substrate interface is therefore smaller in a saturated resistor than in a FET.

In low threshold voltage ($\sim$1 V) devices, the current carrying capability of a saturated resistor is about 2–3 times that of a FET active load of equal width. Hence, a 2–3-times advantage in the backgating effect should be observed. A comparison of the backgating characteristics of the two devices is shown in Fig. 9. The test structure has a 10-μm FET and a 10-μm saturated resistor located 26 μm apart from each other with a 2-μm wide ohmic contact finger located between these two devices serving as a backgating electrode. The normalized saturation currents (measured at $V_{DS} = 2.5$ V) of these two devices are plotted against the negative backgating voltage V_{BG} applied to the ohmic finger. The curves in the figure show that the percentage change in saturation current due to backgating for the FET is about two times higher than the percentage change for the saturated resistor.

The impact of the backgating effect on the circuit performance was again evaluated by using ring oscillators. A wafer which exhibited a strong backgating effect was selected for this experiment. The circuits were tested in the same manner described above; V_{DD} was fixed at 2.2 V and V_{SS} was used as a variable. Tests were carried out at 25°C and 125°C. The results are shown in Fig. 10. Comparison of performance between a circuit with FET pull-up loads and a circuit with saturated resistor loads was made at both temperatures. At 25°C, the circuit with saturated resistor loads is not only faster (smaller τ), but the rate of increase of τ with increasing absolute value of V_{ss} is much lower. This lower sensitivity is attributed to the lower sensitivity of the saturated resistor pull-up loads to the backgating effect of V_{ss}.

Another advantage resulting from less backgating when using saturated resistor loads is less temperature sensitivity. When temperature is increased the backgating effect decreases [7]. At 125°C the propagation delays of both circuits are not sensitive to V_{SS} over a wide voltage range. However, comparing the performance at 125°C and the performance at 25°C, much larger changes in the current values and propagation delay are observed in the circuit with FET pull-up loads. The lower temperature sensitivity of the circuit with saturated resistor pull-ups is not only due to lower backgating, but also to the lower sensitivity of the characteristics of a saturated resistor to temperature. In a FET, the built-in potentials at the Schottky junction and the channel-substrate junction decrease when temperature is increased, causing the threshold voltage and, therefore, the magnitude of the saturation current to increase [8]. In a saturated resistor, where the Schottky junction is not present, the channel-substrate junction is mainly responsible for the change in device characteristics (ignoring mobility changes with temperature). Therefore, the temperature dependence is lower.

C. Reliability

For GaAs FET's, the most common causes for device failure are degradation of ohmic contacts and degradation of Schottky gates [9], [10]. The characteristics of a FET depend strongly on the contact resistance at the source and the drain, and on the properties of the Schottky barrier. For a saturated resistor, the saturation current, as expressed in (1), does not depend on either the contact resistance of the electrodes or the characteristics of the Schottky barrier. Therefore, circuits which use saturated resistors as loads should be more reliable than circuits which use FET active loads.

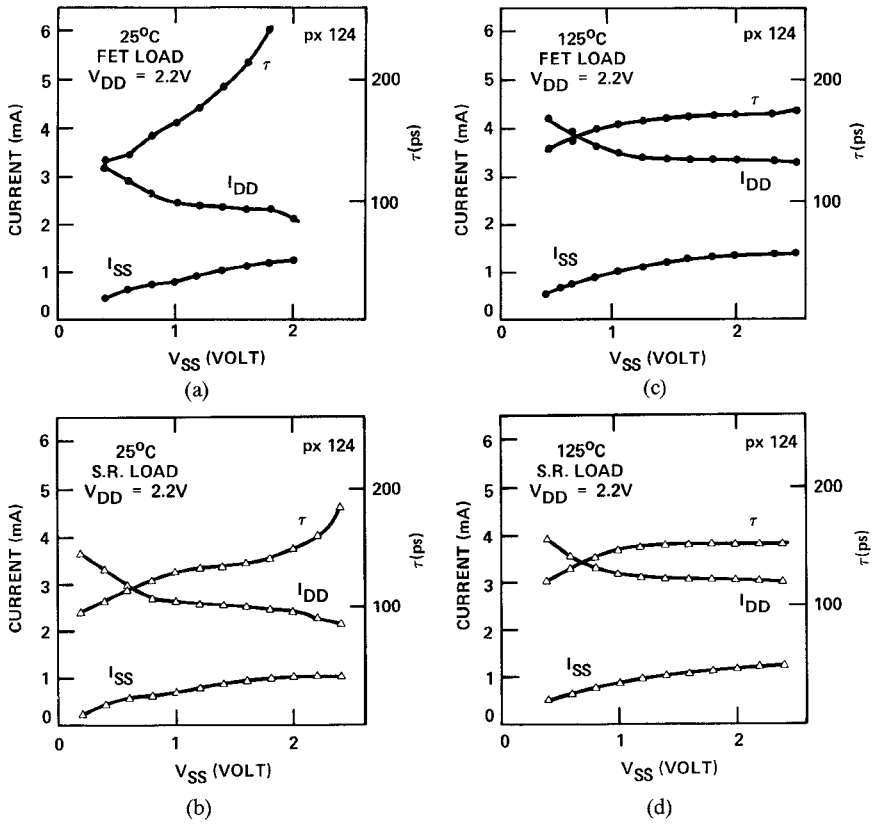


Fig. 10. Performance of ring oscillators with FET pull-up loads (a) and (b), and saturated resistor loads (c) and (d), measured at 25°C (a) and (c), and 125°C (b) and (d).

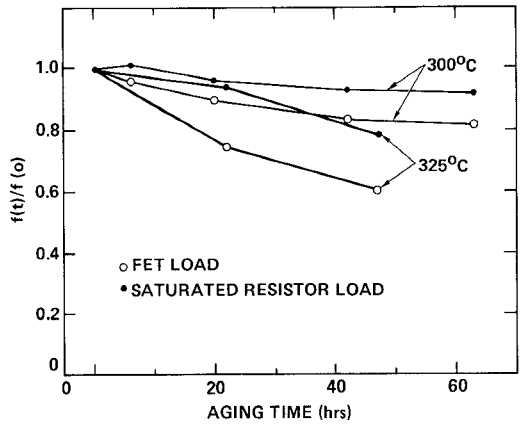


Fig. 11. Reliability of ring oscillators with FET pull-up loads and ring oscillators with saturated resistor pull-up loads. The normalized frequency of oscillator is plotted against aging time.

Accelerated aging test (without bias) on the two types of ring oscillators with different pull-up loads were carried out in order to compare their reliabilities. The circuits were tested before and after aging using fixed bias voltages common to all the circuits and all the tests. The normalized frequency of oscillation versus aging time is plotted in Fig. 11. The open circles correspond to ring oscillators with FET pull-up loads, and the solid dots correspond to ring oscillators with saturated resistor pull-up loads. Each data point in the figure is the average value obtained from 15 circuits. It is shown in the figure that the ring oscillators with saturated resistor loads degrade much slower than the ring oscillators with FET active loads. After aging for 64 h at 300°C, an average of 18-percent degradation in the frequency of oscillation is observed for the circuits with FET active loads, while only 8 percent degradation is observed for the circuits with saturated resistor loads. At 325°C, the degradation rate is higher for both types of circuits, however an advantage factor of about two in the percentage change of the oscillation frequency is again observed for the circuits with saturated resistor loads. By monitoring the currents flowing from the power supplier to the circuits, we found that the frequency degradation of ring oscillators was related to the decrease of the pull-up current I_{DD}. For circuits with FET loads, the I_{DD} decreased with aging time at a much faster rate than the I_{DD} of the circuits with saturated resistor loads. This clearly indicates that the load currents of saturated resistors are much more stable than the currents of the FET's. The degradation of ohmic contacts and Schottky gates contributed to the change in current for FET pull-ups while it had little effect on the current of saturated resistors.

V. Conclusion

A two terminal load device, the saturated resistor, has been fabricated and applied to GaAs integrated circuits. Besides ease of fabrication, it has several advantages over FET active loads. Because of their higher current carrying capability, saturated resistors occupy less area and allow

the fabrication of denser circuits. The uniformity of the saturation current is higher; up to 100-percent improvement has been observed over the FET active load. Circuits fabricated with saturated resistor loads have been shown to be faster and more power saving due to the advantages of no gate capacitance and smaller backgating effect. Finally, circuits designed with saturated resistor loads have been shown to be more reliable.

As GaAs integrated circuits enter into the LSI/VLSI era, the requirements on the device uniformity, circuit performance, and circuit yield are extremely stringent. Over the past few years, a large effort has been put into improvements in material growth [11], wafer processing [12], and ion-implantation techniques [13] in order for GaAs to merge as a viable integrated circuit technology. This work has served to illustrate how improvements in circuit yield, performance, and reliability can also be obtained through the use of saturated resistors independently of material and processing improvements. The use of saturated resistors as load devices should greatly benefit the GaAs integrated circuits in the future.

VI. Acknowledgment

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From 1963 to 1965 he was associated with Westinghouse Electric Corporation, where he was involved in the early development of Si bipolar integrated circuits. Since 1965 he has been employed with Rockwell International and is presently the Project Leader for integrated circuit processing. His areas of research and development have included all phases of ion implantation in both Si and GaAs. Since 1972 he has concentrated on the development of a planar GaAs ion implantation technology. Highlights of his work include the development and fabrication of GaAs FET's, using implanted active layers, and fabrication of the first planar GaAs integrated circuits using multiple localized implantation techniques. He is currently involved with developing planar GaAs integrated circuit processes and responsible for the fabrication of these circuits.

Mr. Welch holds two patents and has numerous publications in the field of ion implantation and its applications.

Mr. Welch is a member of the Electrochemical Society.

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